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Attorney's Docket No.: 07977-052001 / US3053

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Hisashi Ohtani, et al
Serial No. : 08/690,747
Filed : August 1, 1996
Title : METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

Art Unit : 1765
Examiner : Robert Kunemund

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTICE OF DRAWING INCONSISTENCY WITH SPECIFICATION

In response to the Notice of Drawing Inconsistency with Specification (copy attached) mailed June 16, 2004, the following documents are enclosed:

- ☒ A copy of the Date-Stamped Postcard acknowledging receipt of all documents;
- ☒ A copy of the Brief Description of the Drawings; and
- ☒ Drawings (Figs. 9A-9D), as originally filed with the application on August 1, 1996.

Applicants submit that the description of the drawings and the figures, as originally filed, correspond to one another. Accordingly, Applicants request that a patent issue on this application.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 7/16/04

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/690,747	08/01/1996	HISASHI OHTANI	07977/052001	1369

20985 7590 06/16/2004

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EXAMINER	
KUNEMUND, ROBERT M	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 06/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Docketed By Billing Secretary
Due Date: 9/16/04
Deadline: 8/11/04
Initials: CMT

DOCKETED BY PRACTICE SYSTEMS
ACTION CODE: Response IM
BASE DATE: 6-16-04
DUE DATE:
DEADLINE: 7-16-04
INITIALS:

UNITED STATES PATENT AND TRADEMARK OFFICE

UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND
DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

NOTICE OF DRAWING INCONSISTENCY WITH SPECIFICATION

The drawings filed 8-1-96 have been received. However, an inconsistency exists between the drawings and the Brief Description of the Drawings in the specification.

Figures _____ are listed in the Brief Description of the Drawings in the specification but not contained in the Drawings.

Figures 9A-9D are contained in the Drawings but not listed in the Brief Description of the Drawings in the specification.

Applicant is required to correct the above-noted inconsistency within a time period of **ONE MONTH or THIRTY (30) DAYS, whichever is longer,** from the mailing date of this Notice, or within the time remaining in the time period set forth in the Notice of Allowability (Form PTOL-37) to file corrected drawings, whichever is longer. **NO EXTENSION OF THIS TIME PERIOD MAY BE GRANTED UNDER EITHER 37 CFR 1.136 (a) OR (b)**

Failure to correct the above noted inconsistency will result in **abandonment** of the application.

The file will be held in the Publishing Division to await the correction of the inconsistency.

Return Corrected Drawings/Specification to:
Mail Stop Issue Fee
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P.O. Box 1450

Alexandria, VA 22313-1450

Office of Patent Publication/Publishing Division
Customer Service: 703-308-6789
1-888-786-0101

FORM PTO-1631 (REV. 10-03)

08/690747

PATENT
ATTORNEY DOCKET NO.: 07977/052001

The Patent and Trademark Office date stamp sets forth the receipt date (or both the receipt date and the Serial Number) of a patent application identified as follows:

Applicant: Hisashi Ohtani, et al.

Title: METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

[X] Transmittal Letter
[X] Appln 23 Pages of Spec. 5 Pages of Claims 21 Total Claims 1 Pages of Abstract
[ ] Rule 62 Filing Request (FWC) ___ Pages
[X] Assignment & Cover Sheet
[ ] Deposit Account Order Form (2 copies)
[X] Check $ 850 & 40.00 EM020017[illegible]US
[ ] Small Entity Statement
[X] Drawings 99 Sheets Formal ___ Sheets Informal
[X] Combined Declaration and Power of Attorney ✓ signed ___ unsigned
[ ] Preliminary Amendment - ___ Pages
[ ] Information Disclosure Statement
[ ] PTO 1449 Form - ___ Pages
[ ] Prior Art References - Number of References ___
[X] Priority Document - ___ Pages 2, 21, 9, 1, 1, 1, 2, 1, 12, 1, 1
[ ] English Translation
[X] Other Cover sheet

MAILROOM 36 AUG 1 1996 PAT. & TRADEMARK OFF.

Atty/Sec. Initials SCH/KEC Client/Matter Name SEL

Date 8/1/96

COMPLETE WHEN OFFICIAL FILING RECEIPT ARRIVES

- ☐ Serial numbers on the postcard and the filing receipt match.
- ☐ Filing dates on the Express Mail receipt, postcard and the filing receipt match.
- ☐ Filing fee paid by check and the filing fee received on the filing receipt match. If the filing fee was charged to deposit account, the filing fee which should have been charged matches the filing fee received on the filing receipt.
- ☐ Attorney docket numbers on the application, the postcard, and the filing receipt match.
- ☐ Number of sheets of drawings in the application, number noted on the postcard and number noted on the filing receipt match.
- ☐ Total number of claims in the application, noted on the filing receipt, noted in the transmittal letter match.
- ☐ Number of independent claims in the application, noted on the filing receipt, and noted in the transmittal letter match.
- ☐ Attorney named on the filing receipt and attorney named in the declaration/filing request to receive correspondence match.
- ☐ Address of attorney of record is correct and includes "Fish & Richardson".
- ☐ Applicant(s) named on the filing receipt and applicant(s) named in the declaration/filing request match.
- ☐ Title noted on the filing receipt and the title on the application match.
- ☐ Priority date on the filing receipt, delcaration, and transmittal letter match.

Checked By: _____
Practice Systems

RECEIVED AUG 16 1996 FISH & RICHARDSON P.C.

BEST AVAILABLE COPY

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, reference is made of the following detailed description to be read in conjunction with the accompanying drawings, in which:

Figs. 1A-1E schematically show a manufacturing process of a thin-film transistor according to an embodiment of the present invention;

Fig. 2 graphically represents the number of lumps of nickel element contained in a crystalline silicon film per unit area;

Fig. 3 is a photograph for showing the crystalline silicon film;

Figs. 4A-4E schematically indicate a manufacturing step of a thin-film transistor according to another embodiment of the present invention;

Figs. 5A-5D schematically indicates a manufacturing step of a thin-film transistor according to another embodiment of the present invention;

Fig. 6 is a top view for representing a patterning condition of the crystalline silicon film;

Fig. 7 is a top view for indicating a patterning condition of a crystalline silicon film manufactured by the present invention;

Figs. 8A-8D schematically indicate a manufacturing step of a thin-film transistor according to a further embodiment of the present invention; and

Figs. 9A-9D schematically indicate a manufacturing step of a thin-film transistor according to a still further embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS